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EXAMINER	
SELLMAN, CACHET I	
ART UNIT	**PAPER NUMBER**
1762	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,473	PARK, SANG KYUN	
	Examiner	Art Unit	
	Cachet I. Sellman	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-13 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *4-13 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement is made of the amendment filed by the applicant on 3/20/2006, in which claims 1-3 and 14-16 were cancelled, and claim 20 was added. Claims 4-7 and 17-20 are currently pending in U.S. Application Serial No. 10/617,473.

Specification

1. The objections to the specification set forth in paragraphs 6 and 7 of the previous Office Action are withdrawn due to the applicant's submission of an amended specification and abstract where the applicant corrects the abstracts terminology and corrects the typographical errors in the specification.

Drawings

2. The objection to the drawings set forth in paragraphs 8 and 9 of the previous Office Action are withdrawn due to the applicant's submission of replacement drawings and the amendments made to the specification. The drawings were received on 3/20/2006. These drawings are acceptable.

Claim Objections

3. The objection to claims 4 and 17 is withdrawn in light of the applicants amendment correcting the informality.

Response to Arguments

4. Applicant's arguments filed 3/20/2006 have been fully considered but they are not persuasive.

5. In reply to the applicants arguments to the rejection set forth in the previous Office Action where claim 4 is rejected under 35 U.S.C. 103(a) Hoffman (US 6716754 B2) in view of Chen et al. (US 585869). The applicant states compressing a mold that has trenches and via holes into the dielectric layer is not the same as implanting a low dielectric insulating material through the implantation holes of a plate. In the specification the applicant does not define what is meant by implanting the dielectric material through the implantation. The applicant just gives an example of how to perform the step of implanting the dielectric material into the plate. According to The American Heritage Dictionary of the English Language 4th Ed., implant means to 1. Insert or embed an object, 2. To graft or insert a tissue with the body, or 3. To become attached to and embedded. In Merriam Webster implant means 1. To fix or set securely or deeply or 2. To insert in a living site. The examiner believes that when the mold is pressed against the dielectric layer on the substrate and the dielectric layer is forced into the holes of the mold that the dielectric material becomes embedded into the mold and that the dielectric material is set securely or deeply within the holes of the mold which would mean that the dielectric layer is implanted into the holes of the mold therefore the examiner believes that the applicant's arguments that pressing the mold into the dielectric is not the same as implanting are not convincing therefore the rejection as set forth in the previous Office Action is still valid in rejecting claim 4.

6. Applicant's arguments with respect to claims 17-20 have been considered but are moot in view of the new ground(s) of rejection. The applicant amended claim 17 to include the limitation that the first and second insulating material is annealed.

7. In regards to the rejection of claim 17 under 102(e) Hofmann (US 6716754 B2) as set forth in paragraph 15 in the previous Office Action, due to the amendment of the claim adding the limitation that the both insulating materials are annealed after being implanted through the hole the rejection is no longer applicable therefore this rejection is withdrawn.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4-5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann (US 6716754 B2) in view of Chen et al. (US 585869).

Hofmann teaches a method for forming a semiconductor construction where a low dielectric material, which can comprise Cyclotene, is formed on a silicon substrate then trenches are formed in the low dielectric material using contact lithography and a conductive material is formed above the patterned low dielectric material forming lower metal wires (figures 2-7).

Another layer of low dielectric material is formed above the lower metal wires then a mold having a patterned surface comprising projections and valleys between the projections (column 4, lines 16-38 and figure 3) is pressed together with the semiconductor construction to implant the low dielectric material within the mold and once the mold is removed a pattern is formed within the low-k material (column 4, lines 40-51, and figure 4). The low-k dielectric layer contains both shallow trenches and deep openings (column 5, lines 12-15 and figure 6). Upper metal wires are formed which are connected to the lower metal wires through the via holes (figure 11).

Hofmann does not teach annealing the low-dielectric material as required by **claim 4**.

Chen et al. teaches a method for making multilevel electrical interconnections with a low dielectric constant material such as a organic materials, polysilsequioxane (Si polymer), benzocyclobutene (Cyclotene) or a fluorinated polyimide (column 6, lines 16-20), in which a low dielectric constant insulator is annealed at a temperature between 80°C-450°C to cure the organic insulator (column 6, lines 23-25).

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process taught by Hofmann to include the step of annealing the low dielectric material of Chen et al. One would have been motivated to do so because both Hofman and Chen et al. teach processes for forming multilevel interconnect structures using Cyclotene therefore one would have a reasonable expectation of success in forming the interconnect structure with a cured insulator.

Chen et al. teaches using a barrier layer prevents penetration of the metal into other layers (column 5, lines 35-39) as required by **claims 5 and 10**. As stated above the temperature of the mold and the substrate is between 80°C – 450°C as required by **claim 7**. The low dielectric material can be an organic material, polysilsequioxane, or benzocylcobutene, and have a thickness between 2000 and 20000 Angstroms (column 6, lines 16-20) as required by **claim 8**. Chen et al. further teaches that the annealing step can take form 0.5 to 2 minutes as required by **claim 9**.

10. Claims 4-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al in view of Hofmann as applied to claims 17 and 18 above, and further in view of Venkatraman et al. (US 2003/0141499 A1).

Zhao et al. teaches a method for making an interconnect structure using low dielectric constant material. In the method taught by Zhao et al. a low dielectric material is formed on a silicon wafer then a trench is formed and a metal is formed within the trench (column 4, lines 15-25 and figure 1). Another layer of low dielectric material is formed over the conductive layer then dielectric layer is patterned using a photolithography technique; next a dielectric barrier layer is formed then another low dielectric layer is formed and is patterned using photolithography technique (figures 3-9, column 6, lines 10-67). A conductive material is then placed in the via hole therefore forming upper wires that are connected to lower metal wires.

Zhao et al. does not teach using a plate with an engraved pattern for forming a plurality of trenches and via holes onto the silicon substrate or performing an annealing step after implanting the dielectric matieral as required by **claim 4**.

Hofmann discloses a method for forming patterns in low dielectric materials using contact lithography, where a mold having a pattern is pressed into a low dielectric material (abstract). Hofmann teaches that there are numerous difficulties in forming appropriate openings in the insulative material for the redistribution layer as well as the conductive materials but by using the mold to form the pattern will alleviate or eliminate these problems (column 2, lines 12-17). Hofmann further teaches that using contact lithography is advantageous because it can be faster and cheaper than other patterning methods such as photolithographic methods (column 5, lines 29-33).

Venkatraman et al. teaches a process for depositing low dielectric constants and in the process it states that after depositing the low dielectric material it can be annealed to further lower the dielectric constant. Venkatraman et al. further teaches that the annealing must be performed in an inert gas environment, at either atmospheric pressure or under vacuum. Venkatraman et al. further teaches that annealing times vary from 1 minute to 10 hours and the temperature is in the range of 100°C to 500°C.

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process for making a dual damascene interconnect structure taught by Zhao et al. to include using the mold of Hofmann to form vias and trenches in the low dielectric materials. One would have been motivated to do so because both Zhao et al. and Hofmann teach processes for forming semiconductor integrated circuits and Hofman teaches that using the mold to form the patterned semiconductor component is faster and cheaper than

photolithographic methods therefore one would have a reasonable expectation of success in forming the semiconductor component at a faster rate and a lower cost.

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process for forming a dual damascene structure taught by Zhao et al. in view of Hofmann to include the annealing step of Venkatraman et al. in order to form an insulating layer with a low dielectric constant. One would have been motivated to do so because both Zhao et al. in view of Hofmann and Venkatraman et al. teach the use of materials which contain carbon, hydrogen, silicon and oxygen as the low dielectric material therefore one would have a reasonable expectation of success in forming the dual damascene structure with a low dielectric constant material.

Zhao et al. further teaches that a barrier layer is sued to inhibit or prevent copper diffusion into the dielectric layer (column 5, lines 17-19) as required by **claims 5 and 10**. The barrier layer can be formed from cobalt tungsten phosphide using selective electroless deposition (column 10, lines 22-26) as required by **claim 6.** The barrier layer can also be formed of TiN, Ta, TaN, W, WN, SIN, and WSiN (column 5, lines 23-24) using chemical vapor deposition (column 6, line 1) as required by **claims 12 and 13**. As stated above the annealing step is performed at a temperature between 100°C– 500°C and for 1min - 10 hours as required by claims **7 and 9**. The low dielectric material used can be organic materials (polyimides or polymers) or modified SiO_2 materials (fluorinated oxide or silsesquioxane) (column 2, lines 2-7) and is deposited with an approximate thickness of 500-10000 Angstroms (column 6, lines 20-22) as required by **claim 8**. Zhao et al. teaches that the upper and lower wires can consist of a

barrier film and copper film and is formed using a damascene process (Figures 14-16) as required by **claim 11**.

11. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (US 6100184), in view of Hofmann (US 6716754 B2) and Venkatraman et al. (US 2003/0141499 A1).

Zhao et al. teaches a method for making an interconnect structure using low dielectric constant material. In the method taught by Zhao et al. a low dielectric material is formed on a silicon wafer then a trench is formed and a metal is formed within the trench (column 4, lines 15-25 and figure 1). Another layer of low dielectric material is formed over the conductive layer then dielectric layer is patterned using a photolithography technique; next a dielectric barrier layer is formed then another low dielectric layer is formed and is patterned using photolithography technique (figures 3-9, column 6, lines 10-67). A conductive material is then placed in the via hole therefore forming upper wires that are connected to lower metal wires.

Zhao et al. does not teach using a plate with an engraved pattern for forming a plurality of trenches and via holes onto the silicon substrate or performing an annealing step after implanting the first material and the second material as required by **claims 17** or annealing the first and second dielectric for 10 seconds – 10 minutes under anointer gas atmosphere over atmospheric pressure as required by **claims 19 and 20.**

Hofmann discloses a method for forming patterns in low dielectric materials using contact lithography, where a mold having a pattern is pressed into a low dielectric material

(abstract). Hofmann teaches that there are numerous difficulties in forming appropriate openings in the insulative material for the redistribution layer as well as the conductive materials but by using the mold to form the pattern will alleviate or eliminate these problems (column 2, lines 12-17). Hofmann further teaches that using contact lithography is advantageous because it can be faster and cheaper than other patterning methods such as photolithographic methods (column 5, lines 29-33).

Venkatraman et al. teaches a process for depositing low dielectric constants and in the process it states that after depositing the low dielectric material it can be annealed to further lower the dielectric constant. Venkatraman et al. further teaches that the annealing must be performed in an inert gas environment, at either atmospheric pressure or under vacuum. Venkatraman et al. further teaches that annealing times vary from 1 minute to 10 hours and the temperature is in the range of 100°C to 500°C.

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process for making a dual damascene interconnect structure taught by Zhao et al. to include using the mold of Hofmann to form vias and trenches in the low dielectric materials. One would have been motivated to do so because both Zhao et al. and Hofmann teach processes for forming semiconductor integrated circuits and Hofman teaches that using the mold to form the patterned semiconductor component is faster and cheaper than photolithographic methods therefore one would have a reasonable expectation of success in forming the semiconductor component at a faster rate and a lower cost.

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the process for forming a dual damascene structure taught by Zhao et al. in view of Hofmann to include the annealing step of Venkatraman et al. in order to form an insulating layer with a low dielectric constant. One would have been motivated to do so because both Zhao et al. in view of Hofmann and Venkatraman et al. teach the use of materials which contain carbon, hydrogen, silicon and oxygen as the low dielectric material therefore one would have a reasonable expectation of success in forming the dual damascene structure with a low dielectric constant material.

In claim 17, the applicant does not require that the plate be removed after the two insulating materials is implanted into the holes (does not have to occur in sequential order) therefore, placing the mold over the first dielectric layer, implanting the dielectric layer into the mold, removing the mold, forming the barrier layer, pressing the mold so that the barrier layer is implanted into the mold then removing the plate would meet the limitation of "implanting a first insulating material through the first implantation hole; implanting a second insulating material through the second implantation hole; then removing the plate. Also the claim states comprising the steps meaning additional steps can occur therefore when implanting a second insulating material through the second implantation hole can mean to use a different plate with first and second implantation holes can be used to pattern the second insulating material.

Hofmann further teaches that low dielectric materials are those that have a dielectric constant below 3.5 (column 1, lines 52-55). Zhao et al. further teaches that chemical-mechanical polishing is used to polish away the excess conductive material above the trench

level and the dielectric layer functions as a polish-stop layer (column 8, lines 56-60; figure 11) as required by **claim 18**.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cachet I. Sellman whose telephone number is 571-272-0691. The examiner can normally be reached on Monday through Friday, 7:00 - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cachet Sellman
Patent Examiner
AU 1762

TIMOTHY MEEKS
SUPERVISORY PATENT EXAMINER